



TM  
AT/2812

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

application of

ENNIS T. OGAWA ET AL.

Serial No. 10/662,302 (TI-33455.10)

Filed September 16, 2003

For: VERSATILE SYSTEM FOR DIFFUSION LIMITING VOID FORMATION

Art Unit 2812

Examiner Andre C. Stevenson

Customer No. 23494

Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8**

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

10-3-05  
J. M. Cantor

Jay M. Cantor, Reg. No. 19,906

Sir:

**BRIEF ON APPEAL**

**REAL PARTY IN INTEREST**

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

**RELATED APPEALS AND INTERFERENCES**

There are no known related appeals and/or interferences.

## **STATUS OF CLAIMS**

This is an appeal of claims 15 to 35, all of the rejected claims. No claims have been allowed, and the subject matter of cancelled claims 1 to 14 is now Patent No. 6,737,351. Please charge any costs to Deposit Account No. 20-0668.

## **STATUS OF AMENDMENTS**

An amendment was not filed after a second final rejection.

## **SUMMARY OF CLAIMED SUBJECT MATTER**

The claimed invention relates to a semiconductor device structure to decrease diffusive damage effects to a location within a primary structure, such as, for example, a first interconnect 402, 502, 602. The primary structure will have an *active diffusion volume* 410, 514, 612 which is determined relative to a location 406, 506, 606 within the primary structure wherein voids can be located. The terms “active diffusion volume” are defined at page 17, lines 7 to 9 as “the smallest overlapping portion of the three volumes surrounding a vulnerable SIV [stress induced voids] site”. One or more redundant structures 408, 508 are disposed within the active diffusion volume to minimize movement of voids to the location. The number of redundant structures disposed within the active diffusion volume can be determined by calculating, based upon the active diffusion volume, a potential diffusive damage to the location in the primary structure, determining, based on the potential diffusive damage, a desired number of redundant structures to be disposed and disposing the desired number of redundant structures within the active diffusion volume. The redundant structure can be operative relative to diffusive redundancy only or relative to electrical redundancy. A desired geometric orientation of the desired number of redundant structures can be determined with respect to the location. A copper-based, dual-

damascene structure is provided, an active diffusion volume within the dual-damascene structure is determined relative to a location within the dual-damascene structure to which voids can migrate and a redundant structure is disposed within the active diffusion volume to minimize movement of voids to the location. A second interconnect 404, 504, 604 can overlap and be coupled to the first interconnect through the redundant structure 408 as well as through the location 406, 506. The redundant structures(s) can be a via(s). The structure can be at least one electrically insulating slot 608, 610 disposed in the first layer and within the active diffusion volume. A buffer structure (vias 408, 508, page 27, lines 8 to 26) is disposed upon the second metallic interconnect in proximity to the primary via structure and within the diffusion volume to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the second metallic interconnect. The buffer structure can include a second, electrically inactive, via structure, disposed upon the second metallic interconnect proximal to the primary via structure and within the active diffusion volume or an electrically inactive structure disposed upon the second metallic interconnect to immediately and completely surround the primary via structure.

### **GROUNDS OF REJECTION**

Claims 15 to 35 were rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (U.S. 6,468,894).

### **ARGUMENT**

A rejection under 35 U.S.C. 102(e) requires that each and every feature of a claims and each and every function of that feature be found in a single reference. This is not the case herein.

Claim 15 requires, among other features, a second metallic interconnect having a primary via structure, the primary structure having an active diffusion volume relative to a location within the primary structure wherein voids can be located disposed between and electrically intercoupling the first and second metallic interconnects and a buffer structure, disposed upon the second metallic interconnect in proximity to the primary via structure and within the diffusion volume to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the second metallic interconnect. The terms “active diffusion volume” are defined in the specification at page 17, lines 5 to 9, “by the simultaneous intersection of the interconnect volume diffusion volume, and stress gradient region at a specific site within a device structure. Hence, ‘active diffusion volume’ is the smallest overlapping portion of the three volumes surrounding a vulnerable SIV [stress-induced voiding] site”. An example is provided in Fig. 3 and discussed on page 17, lines 10ff. No such structure is taught or even remotely suggested by Yang et al. While Yang et al. shows multiple and dummy vias, nowhere is there a teaching or suggestion to place these vias in the manner claimed. In fact, Yang et al. does not even mention the problem or SIV and utilized the dummy vias as stated in the ABSTRACT-- to increase the mechanical strength of the via layer and increase the resistance to delamination and scratching during chemical mechanical polishing or CMP.

It is initially noted that claim 15 requires “a buffer structure disposed upon the second metallic interconnect in proximity to the primary via structure and within the diffusion volume to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the second metallic interconnect”. The term “active diffusion volume” as defined herein, is the smallest overlapping portion of the three volumes surrounding a vulnerable SIV site (see page 17, first full paragraph). It is noted that the rejection is based upon

35 U.S.C. 102. Accordingly, it is imperative that the examiner clearly demonstrate that the claimed subject matter is found in Yang et al. Not only has this not been done, but, in addition, no such structure is found in Yang et al. An “active diffusion volume” as defined in the specification, which is the lexicon for the subject application, is nowhere taught or even remotely suggested by Yang et al. This conclusion is further evidenced by the fact that Yang et al. does not discuss or even hint at the problem involved, let alone the solution as set forth herein. There is nothing inherent in Yang et al. which relates to the present invention other than the cavalier statement of the examiner.

The feature discussed above with reference to claim 15 is also found in independent claims 21 and 29 wherein, in each claim, a redundant structure is disposed within the active diffusion volume (claim 21) and a structure to minimize migration of the voids toward the via is disposed in the first layer having an active diffusion volume.

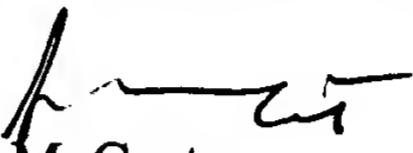
Each of the dependent claims defines patentably over Yang et al. for the reasons stated above with reference to the claims from which they depend.

In addition, since the rejection is based upon section 102, the examiner has not shown how each of the features claimed in each of the dependent claims is specifically found in Yang et al.

## CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



Jay M. Cantor  
Reg. No. 19906  
(301) 424-0355  
(972) 917-5293

## **CLAIMS APPENDIX**

The claims on appeal read as follows:

15. A semiconductor device structure comprising:

a first metallic interconnect;

a second metallic interconnect having a primary via structure, said primary structure having an active diffusion volume relative to a location within the primary structure wherein voids can be located, disposed between and electrically intercoupling the first and second metallic interconnects; and

a buffer structure disposed upon the second metallic interconnect in proximity to the primary via structure and within the diffusion volume to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the second metallic interconnect.

16. The structure of claim 15 wherein the first metallic interconnect and the primary via structure are copper-based dual damascene structures.

17. The structure of claim 15 wherein the buffer structure comprises a second via structure, disposed between and electrically intercoupling the first and second interconnects.

18. The structure of claim 15 wherein the buffer structure comprises a second, electrically inactive, via structure, disposed upon the second metallic interconnect proximal to the primary via structure and within the active diffusion volume.

19. The structure of claim 18 wherein the buffer structure comprises an electrically inactive structure disposed upon the second metallic interconnect to immediately and completely surround the primary via structure.

20. The structure of claim 15 wherein the buffer structure comprises:

- a second via structure, disposed between and electrically intercoupling the first and second metallic interconnects; and
- a third electrically inactive, via structure, disposed upon the second metallic interconnect proximal to the primary via structure.

21. A semiconductor device for decreasing diffusive effects to a location within a primary structure, comprising:

- a primary structure having an active diffusion volume relative to a location within the primary structure where voids can be located; and
- a redundant structure within the active diffusion volume to minimize movement of voids to said location.

22. The device of claim 21 wherein the redundant structure comprises plural redundant structures.

23. The device of claim 21, wherein the redundant structure is operative relative to diffusive redundancy only.

24. The device of claim 21 wherein the redundant structure is operative relative to electrical redundancy.

25. The device of claim 21 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate.

26. The device of claim 22 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate.

27. The device of claim 23 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate.

28. The device of claim 24 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate.

29. A semiconductor device to minimize diffusive damage effects comprising:  
a first layer of interconnect material and a second layer of interconnect material partially overlapping said first layer of interconnect material and coupled to said first layer of interconnect material by a via;  
an active diffusion volume in said first layer of interconnect material within which voids can be located; and  
a structure in said first layer within said active diffusion volume to minimize migration of said voids toward said via.

30. The device of claim 29 wherein said structure is at least one via extending from said first layer and spaced from said second layer.

31. The device of claim 30 wherein said at least one via is a plurality of vias.

32. The device of claim 31 wherein said plurality of vias are equidistant from said via and spaced apart.

33. The device of claim 29 wherein said structure is at least one electrically insulating slot disposed in said first layer and within said active diffusion volume.

34. The device of claim 24 wherein said at least one slot is a plurality of spaced apart slots.

35. The device of claim 29 wherein said structure further includes at least one electrically insulating slot disposed in said first layer and within said active diffusion volume.

**EVIDENCE APPENDIX**

Not applicable

**RELATED PROCEEDINGS APPENDIX**

Not applicable